REMARKS

Claims 1-28, all the claims pending in the application, stand rejected upon informalities and on prior art grounds. Claims 1-28 stand rejected upon informalities under 35 U.S.C. §112, first paragraph. Claims 3-4, 10-11, and 18-19 stand rejected upon informalities under 35 U.S.C. §112, second paragraph. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. §112 Rejections

A. The rejection of claims 1-28 under 35 U.S.C. §112, first paragraph.

The Applicants respectfully disagree with the position that support is not found in the specification for the language "wherein said target spacer width controls an amount of diffusion of said dopant into a channel region of said substrate below said gate conductor", which was previously amended into independent Claims 1, 9, 16, and 14.

Specifically, paragraph [0004] explains that "implanting dopants with a sufficient energy to dope the source/drain regions and for halo formation using the polygate as a self-aligned mask can cause the dopants to penetrate through the poly gate and the gate dielectric into the channel as the gate height is decreased". Thus, with regard to the claimed invention, paragraph [0039] indicates that "the sacrificial layers 14-16 allows a sufficiently high-energy-implantation ... to be utilized for doping not only the gate but also the source, drain, and halo regions without impurity penetration through the gate oxide 12 into the channel region of the silicon 11." Additionally, paragraph [0005] explains that "with a shorter gate height, the maximum size of the spacer is reduced ...,

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resulting in lateral encroachment of S/D dopants and a higher probability of silicide bridging between the gate and the S/D." Thus, paragraph [0030] indicates that the "sacrificial layer at the top of the gate stack allows the formation of larger disposable spacers", that the "invention uses a two-step spacer formation process for spacer width modulation..." and that "[w]ith the larger spacers, the invention also avoids the dopant encroachment... problems that can occur when the reduced gate height limits and decreases the achievable size of the spacers...". Furthermore, paragraph [0031] specifically discusses that the "width of the spacer is made relatively larger" ... in order to give more room for boron diffusion" and that "larger disposable spacers" are used to "minimize any effects of lateral encroachment of boron". Paragraph [0050] provides that without the sacrificial layers, the "gate height would make it difficult to form a disposable spacer large enough to separate the raised source/drain regions from the gate sidewall." Lastly, paragraph [0036] actually refers to the "target spacer width" as a design element of the invention.

Therefore, while the specification does not explicitly state that the target spacer width controls an amount of diffusion of said dopant (or impurities) etc., this feature would be implicitly understood by one skilled in the relevant art given the above-cited information contained in the specification. However, to further clarify this feature of the invention, as disclosed in the specification, claim 1 is amended to reflect "doping regions of said substrate not protected by said spacers with a dopant to form source and drain regions adjacent said gate stack, wherein said target spacer width avoids lateral encroachment of said dopant through said substrate to below said gate stack." Similarly,

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claims 9, 16 and 24 are amended to reflect "implanting impurities into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width avoids lateral encroachment of said impurities through said substrate to below said gate stack."

Each of the features of the amended claims 1, 9, 16 and 24 are supported by the specification language cited-above. Furthermore, no new matter is presented by the amended claim language in that the feature "wherein said target spacer width avoids lateral encroachment of said dopant through said substrate to below said gate stack" of claim 1 and similar language in claims 9, 16 and 24 reflect the same matter as in the previously presented feature of "wherein said target spacer width controls an amount of diffusion of said dopant [or impurities] into a channel region of said substrate below said gate conductor." In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections of claims 1-28.

B. **The rejection of claims 3-4, 10-11, and 18-19 under 35 U.S.C. §112, second paragraph.**

Claims 3-4, 10-11, and 18-19 are amended herein to address instances of indefiniteness.

II. The Prior Art Rejections

Claims 1-28 again stand rejected under 35 U.S.C. §102(b) as being anticipated by

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Park, et al. (U.S. Patent No. 6,429,084), hereinafter referred to as Park. Applicants respectfully traverse these rejections based on the following discussion.

Regarding independent claim 1, Park does not teach or suggest "doping regions of said substrate not protected by said spacers with a dopant to form source and drain regions adjacent said gate stack, wherein said target spacer width avoids lateral encroachment of said dopant through said substrate to below said gate stack." Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest "after said epitaxially growing of said raised source and drain regions, implanting impurities into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width avoids lateral encroachment of said impurities through said substrate to below said gate stack."

As discussed in the July 18, 2005 amendment, the cited prior art and the present invention each provide methods for forming CMOS transistors with raised source and drain regions and each address problems associated with reduced height of gate conductors; however, the problems addressed are different as are the processes used to solve the problems.

Specifically, Park addresses the problem of unwanted overgrown epi growth on the gate and STI but not unwanted diffusion of dopants. Park discloses a method of forming CMOS transistors with raised source and drain regions (col. 1, lines 5-6) in

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which a protective layer is provided over the gate and the STI (col. 1, lines 26-29). In the Park method a gate stack is formed with several sacrificial layers above a gate conductor (col. 1, lines 58-62). The sacrificial layers protect the surface of the gate conductor during subsequent processing. A protective nitride layer is deposited over the substrate, gate stack, and the STI structures (col. 1, lines 66-67). Temporary spacers are formed against the gate stack and a width of the spacers is "set to define the area for the halo and extensions implants" (col. 2, lines 1-5). A portion of the nitride layer 60 is etched to above the substrate to define the source and drain regions and the temporary spacers are removed (col. 2, lines 25-30). Then, the source and drain regions in the substrate are implanted (col. 2, lines 33-34; see Figure 5). Column 2, lines 34-37 provide that "the layer 60 is thick enough to block the implant in the region that will contain the extension implant." After the source and drain regions in the substrate are implanted, raised source and drain regions are epitaxially grown (col. 2, lines 43-47; see Figure 7). Unwanted epi growth is prevented by the remaining nitride layer. Then, after additional processing steps, extension and halo implantation is performed (col. 2, lines 48-64), which also implants the raised epitaxially grown source and drain regions.

Park mentions (at col. 2, lines 34-37) that the thickness of the nitride layer 60 is sufficient to "*block the implant in the region that will contain the extension implant.*" However, Park *does not* address the issue of lateral encroachment of source/drain dopants through the substrate into the channel region below the gate conductor. Specifically, the height of the temporary spacers in Park is not discussed at all and the width of the temporary spacers in Park is set in order to define the distance that the nitride layer will

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extend out from the gate conductor and thus to "define the area for the halo and extensions implants" (col. 2, lines 1-5). Park indicates that this nitride layer is thick enough to block penetration by the dopant into the substrate (col. 2, lines 34-37), however, the distance that the nitride layer extends from the gate stack is considered only for purposes of defining the extensions implant. This distance (which is offered as disclosing the target spacer width of the present invention) is not selected by Park in order to avoid diffusion of the source/drain dopants through the substrate towards the gate stack and into the channel region (i.e., lateral encroachment of the dopants).

Additionally, the Office Action further refers to the fact that the Park drawings do not illustrate impurities under the gate conductor as support for the position that the temporary spacers in Park protect the channel region. However, since the Park drawings do not illustrate any lateral diffusion of the source/drain dopants and since those skilled in the art would recognize that such lateral diffusion would necessarily occur, especially following the epi growth process, the lack of dopants in the extension region and under the gate stack in the Park drawings does not support the position that the spacers of Park protect the channel region but rather further illustrates that Park did not consider lateral diffusion when determining the spacer width.

Therefore, the Applicants respectfully submit that Park does not teach or suggest forming spacers with a target spacer width (see paragraph [0036]), "wherein said target spacer width avoids lateral encroachment of said dopant through said substrate to below said gate stack" (see paragraphs [0030-0031] and [0039], as claimed in claim 1, or "wherein said target spacer avoids lateral encroachment of said impurities through said

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substrate to below said gate stack," as claimed in claims 9, 16, and 24 (see paragraphs [0029-0031] and [0039]).

Furthermore, regarding independent claims 9, 16 and 24, Park does not teach or suggest "after said epitaxially growing of said raised source and drain regions, implanting said impurities into said raised source and drain regions and into said substrate below said raised source and drain regions, wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process" (see paragraphs [0042] and [0047]). Specifically, Park discloses implanting the source and drain regions in the substrate *before growing the epi* (col. 2 lines 33-48, see Figure 5). The impurities implanted into these source and drain regions in the substrate would necessarily be subjected to the epi process (col. 2, lines 44-48, see Figure 7) with a conventional temperature range from about 750°C-850°C) and, thus, subjected to the deleterious effects of transient enhanced diffusion of impurities, such as boron. Col. 2, lines 56-58 and associated Figures 9-10 of Park disclose that after the epi is grown a second implant process is used to implant dopants into the halos, extensions and a section of the epi, but not into the source and drain regions in the substrate below the epi (which were previously implanted).

Regarding independent claim 16, Park further does not teach or suggest "wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities". Contrarily, as mentioned above, Park teaches doping the source and drain regions in the substrate prior to growing the epi on those source and drain regions (see Figures 5-7 and associated text in the Specification). Thus, Park

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necessarily teaches that the process of epitaxially growing the raised source and drain regions is performed in the presence of doping impurities.

Therefore, the Applicants respectfully submit that independent claims 1, 9, 16, and 24 are patentable over the prior art of record. Further, dependent claims 2-8, 10-15, 17-23 and 25-28 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

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Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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